

FIG. 1

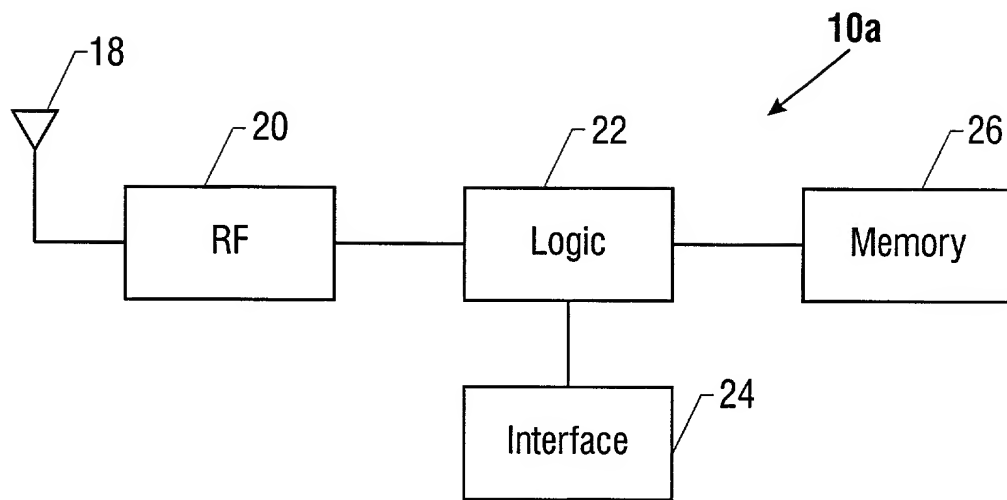


FIG. 2

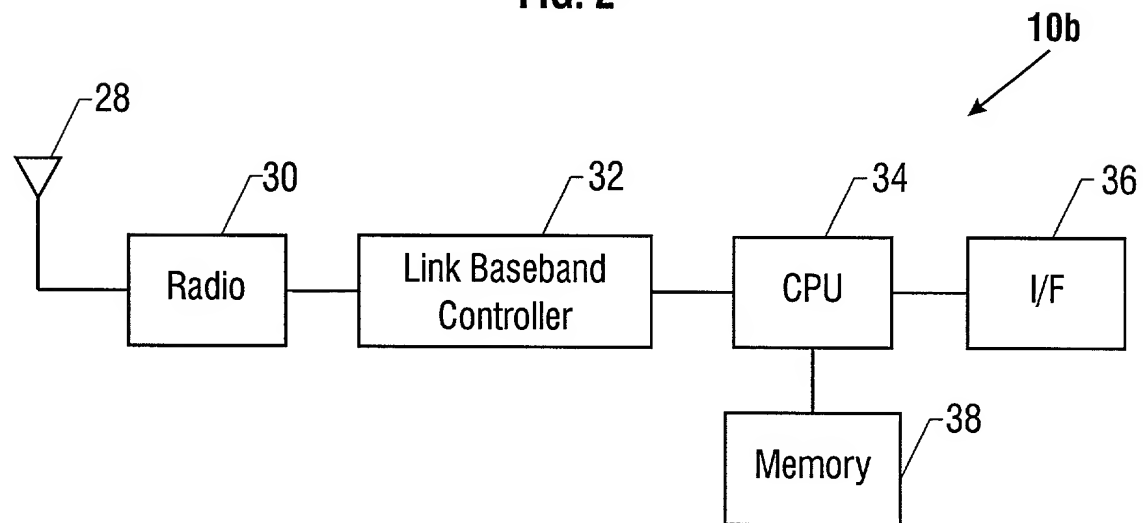


FIG. 3

FIG. 4 is a cross-sectional view of a semiconductor device in accordance with the present invention. The device includes a substrate 40, a p-type region 42, an n-well 44, a p-well 46, and a gate stack 48. The gate stack 48 is formed on the p-type region 42 and the n-well 44. The p-well 46 is formed in the p-type region 42. The n-well 44 is formed in the p-type region 42. The gate stack 48 is formed on the p-type region 42 and the n-well 44. The gate stack 48 is formed on the p-type region 42 and the n-well 44.

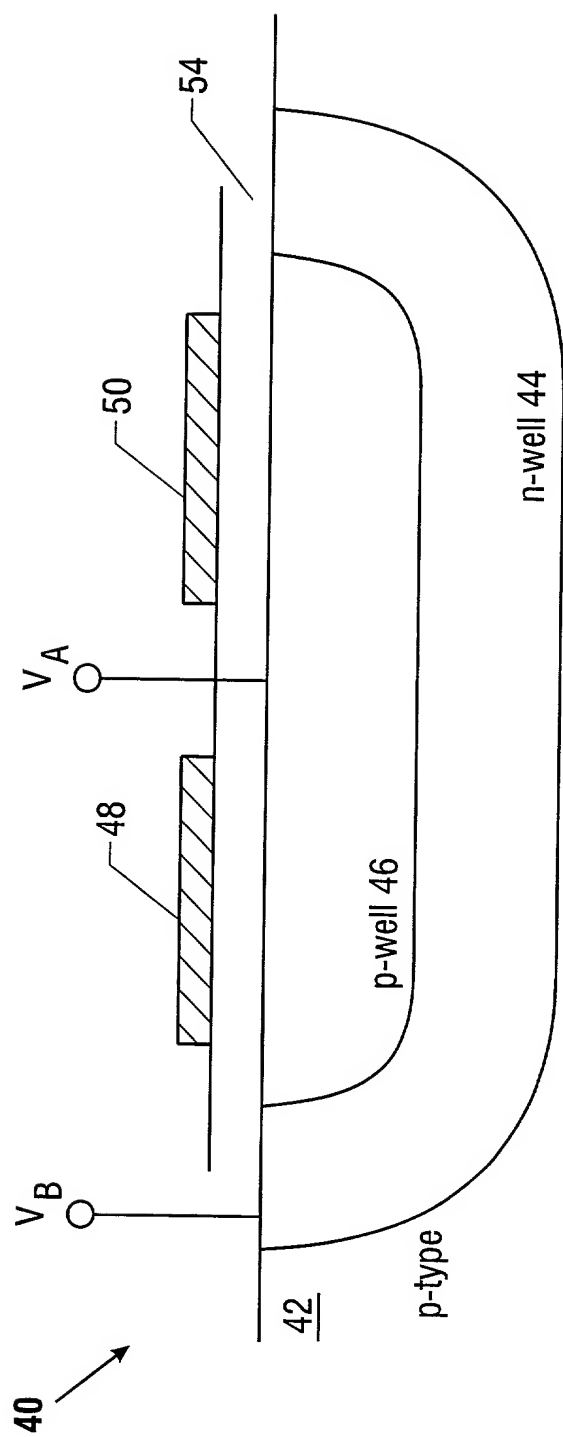
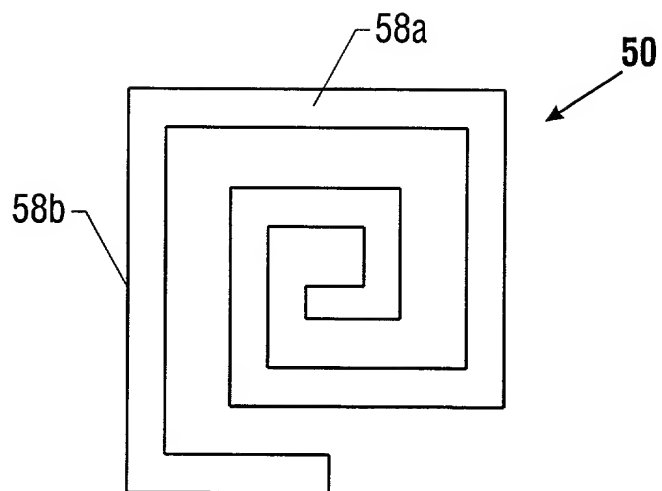
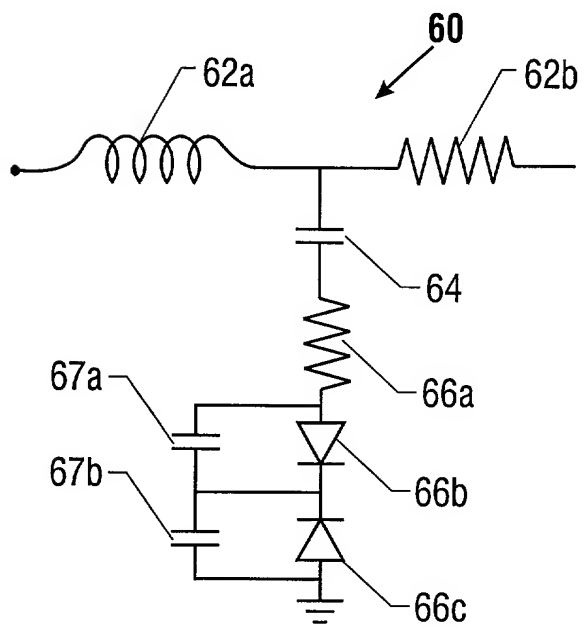


FIG. 4

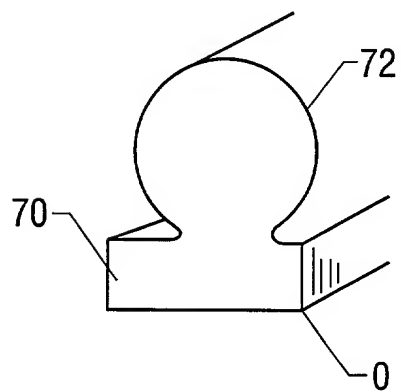
**FIG. 5**



**FIG. 6**



**FIG. 7**



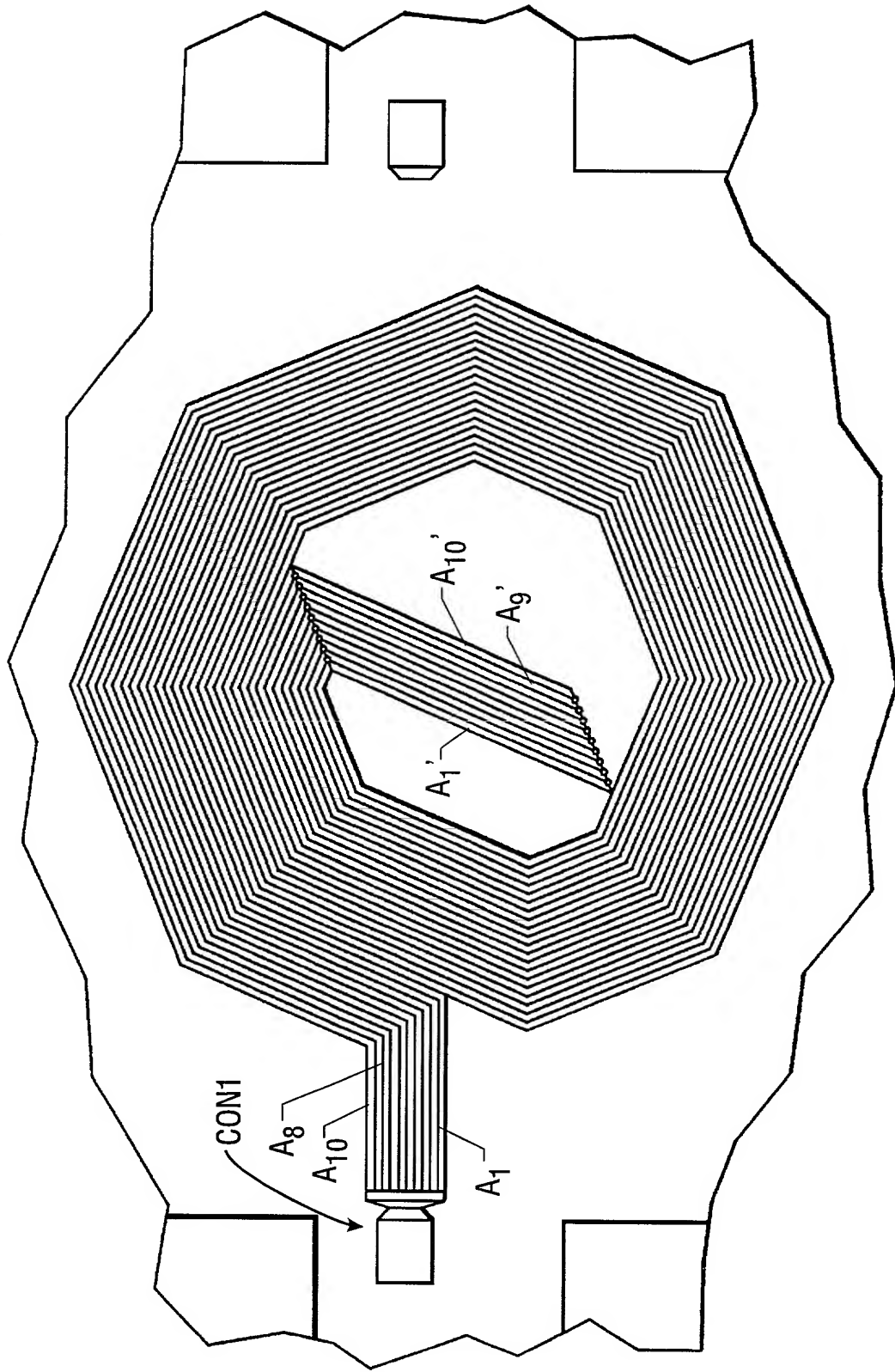


FIG. 8A

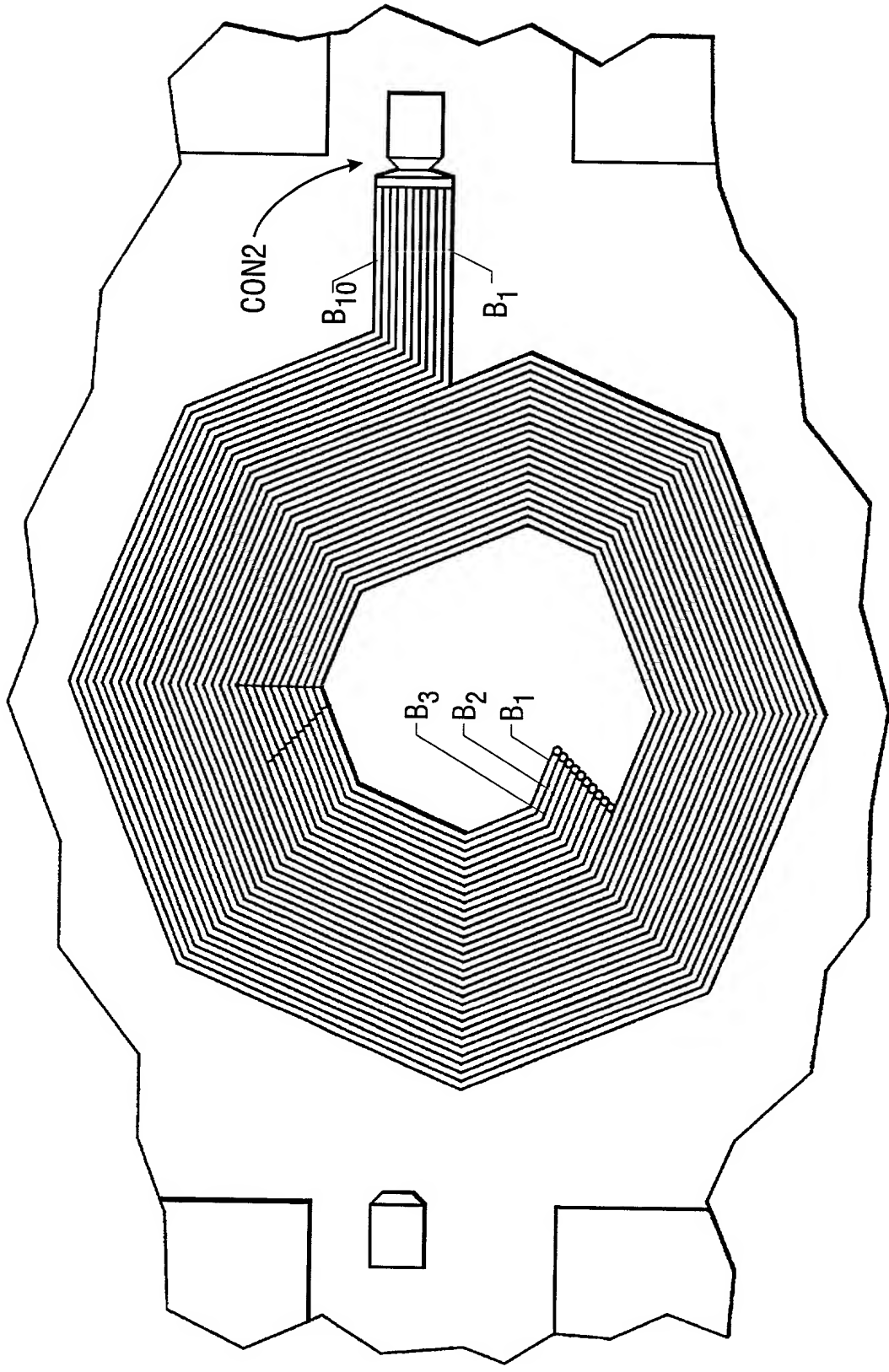


FIG. 8B

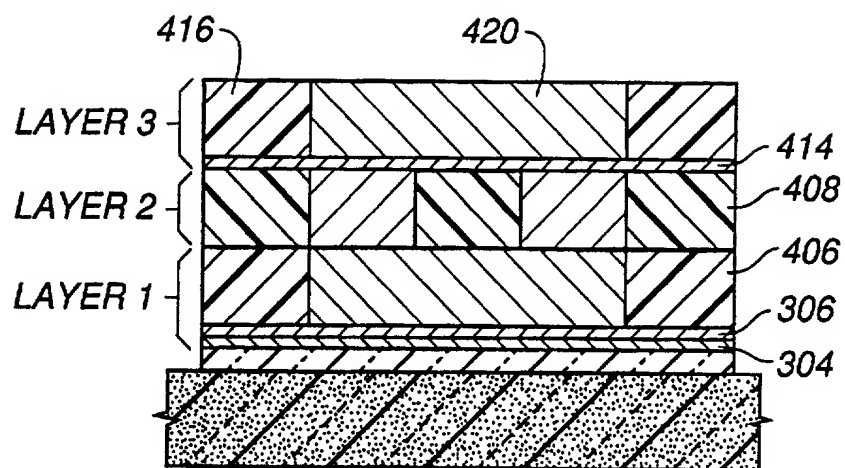


FIG. 9

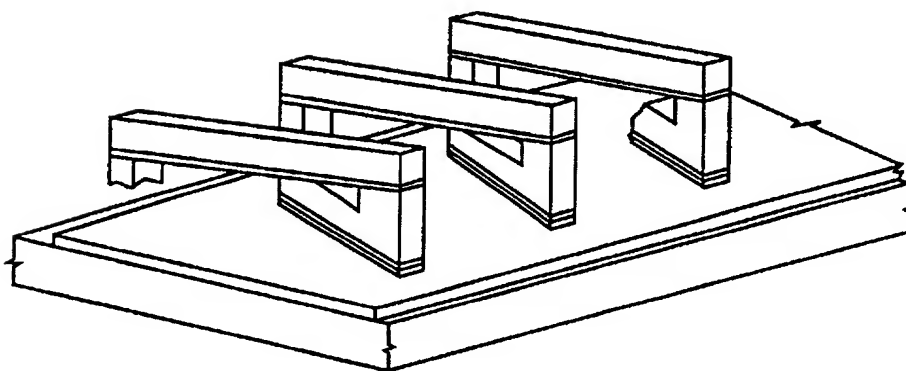


FIG. 10

450

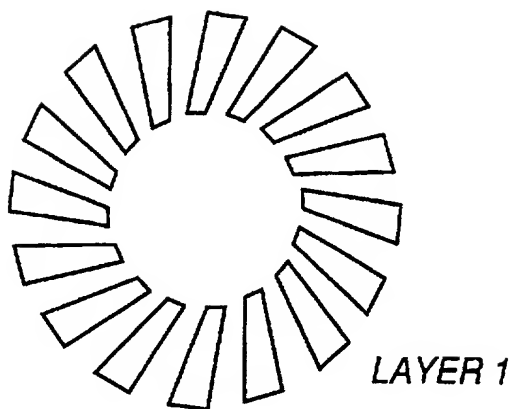


FIG. 11

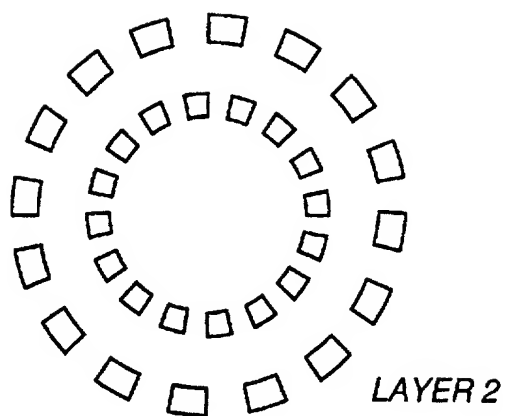


FIG. 12

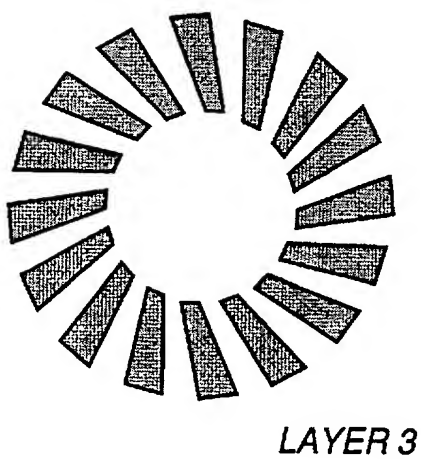


FIG. 13

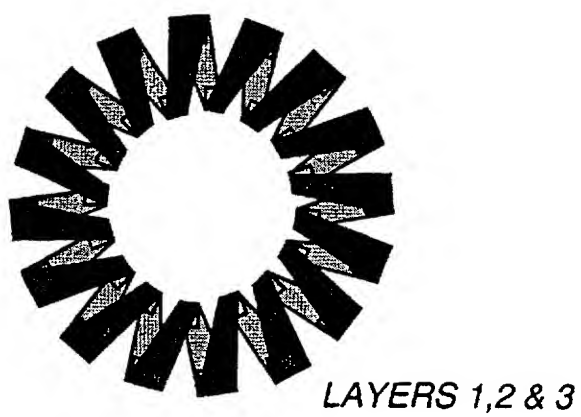
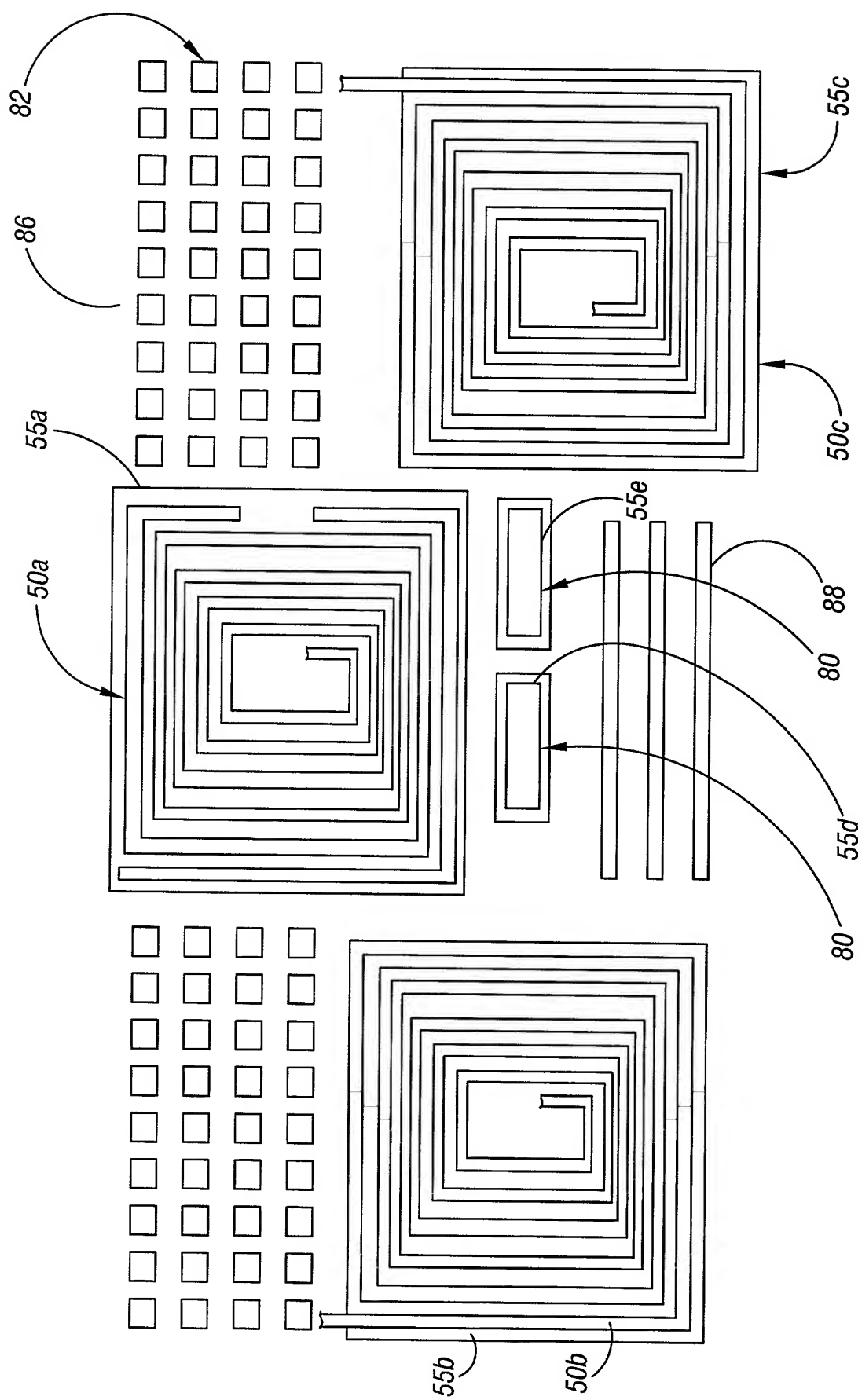
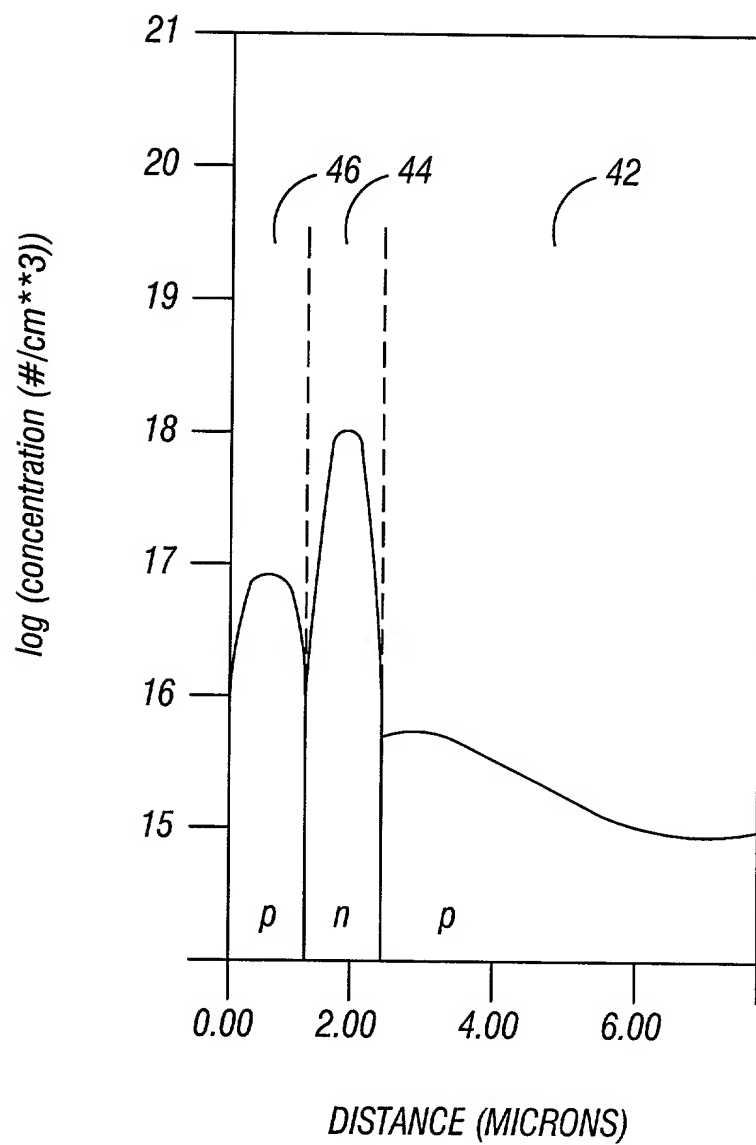


FIG. 14

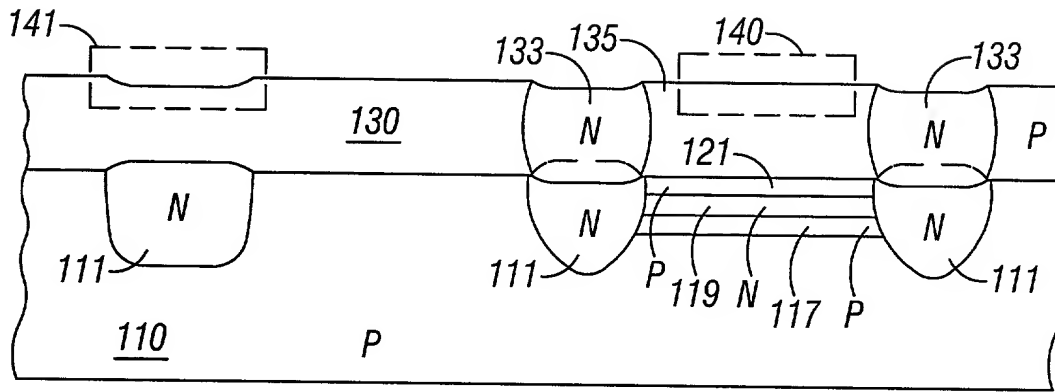


**FIG. 15**

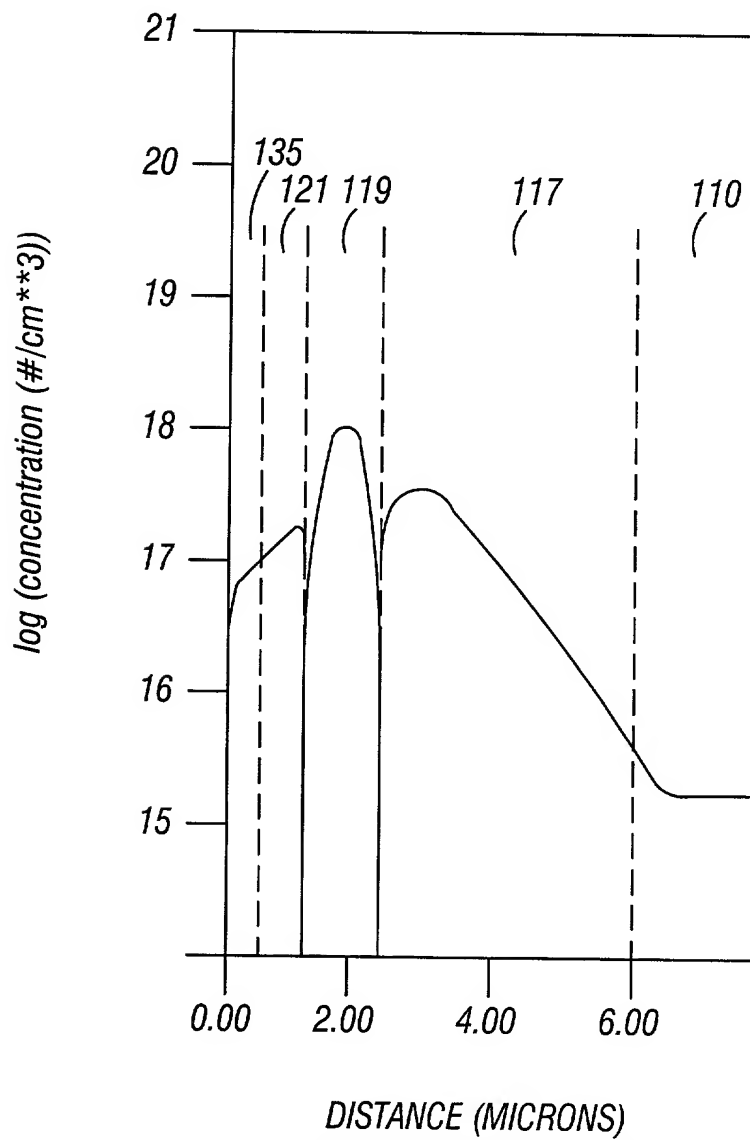




**FIG. 16**



**FIG. 17 (PRIOR ART)**



**FIG. 18 (PRIOR ART)**

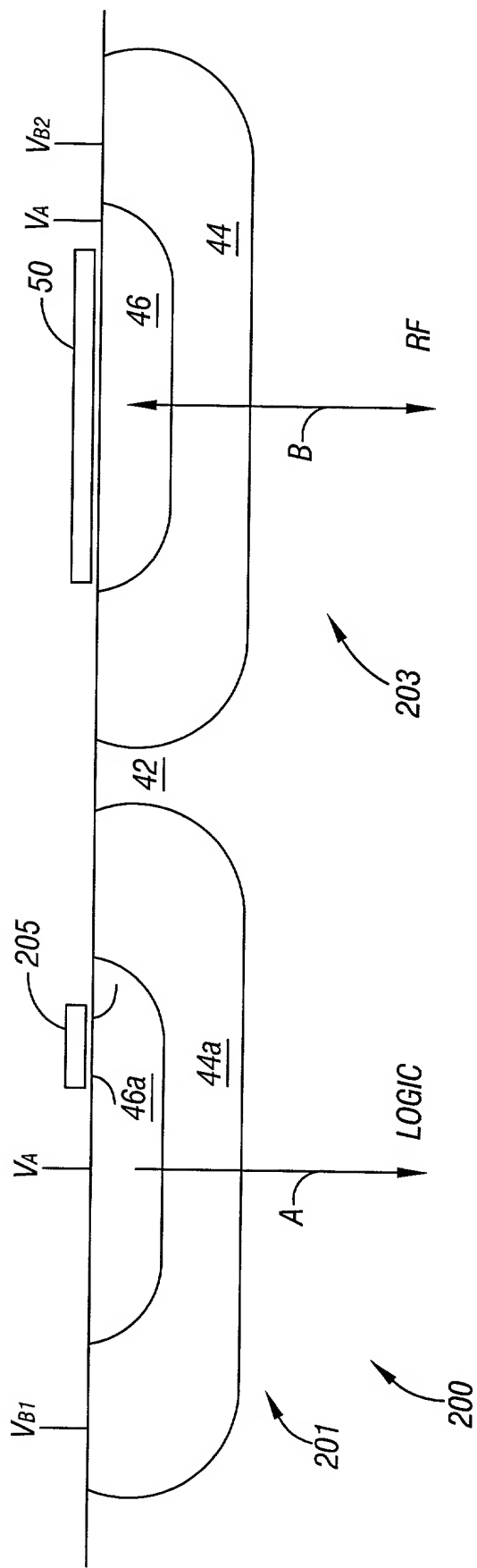


FIG. 19

200

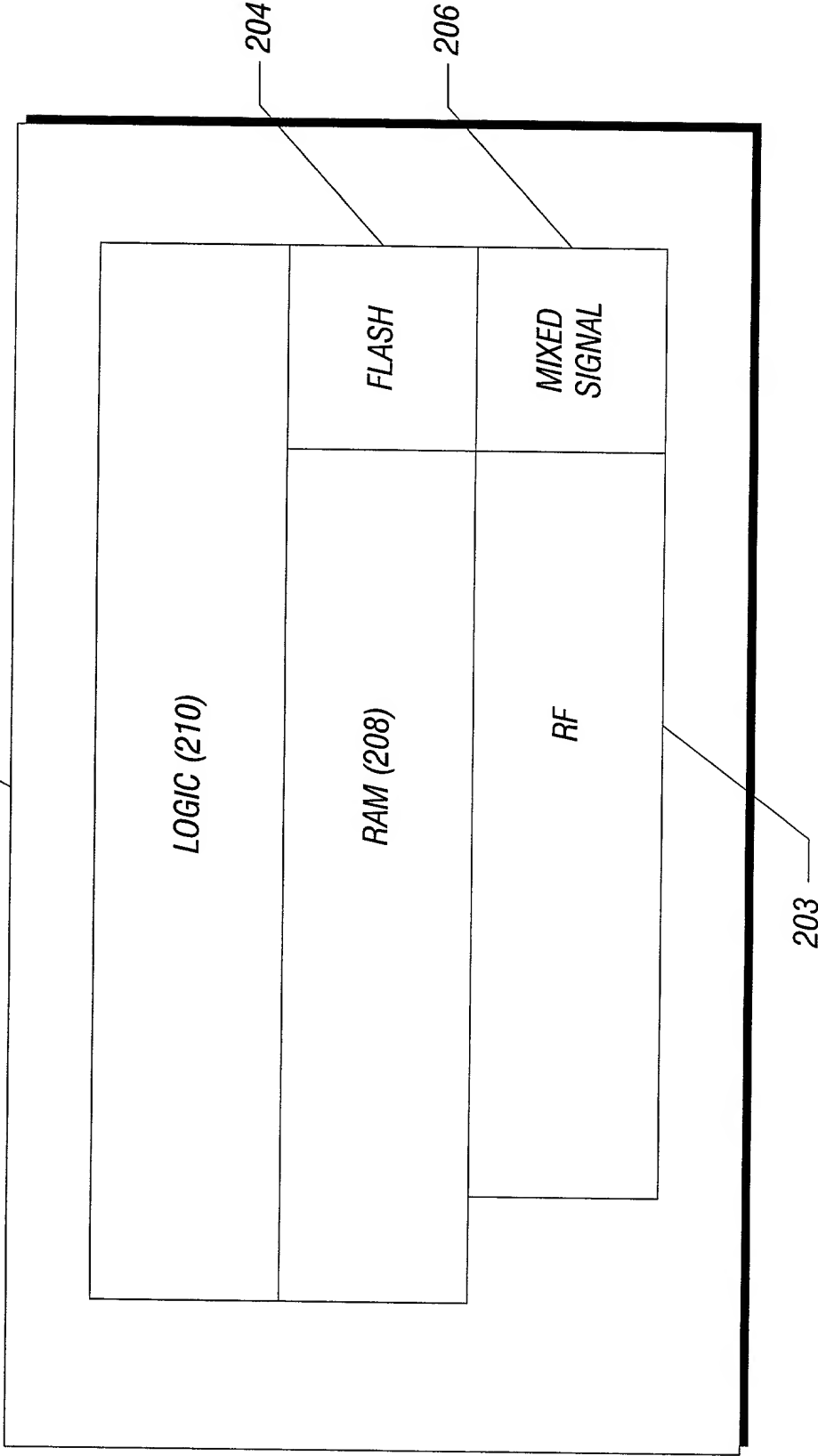


FIG. 20

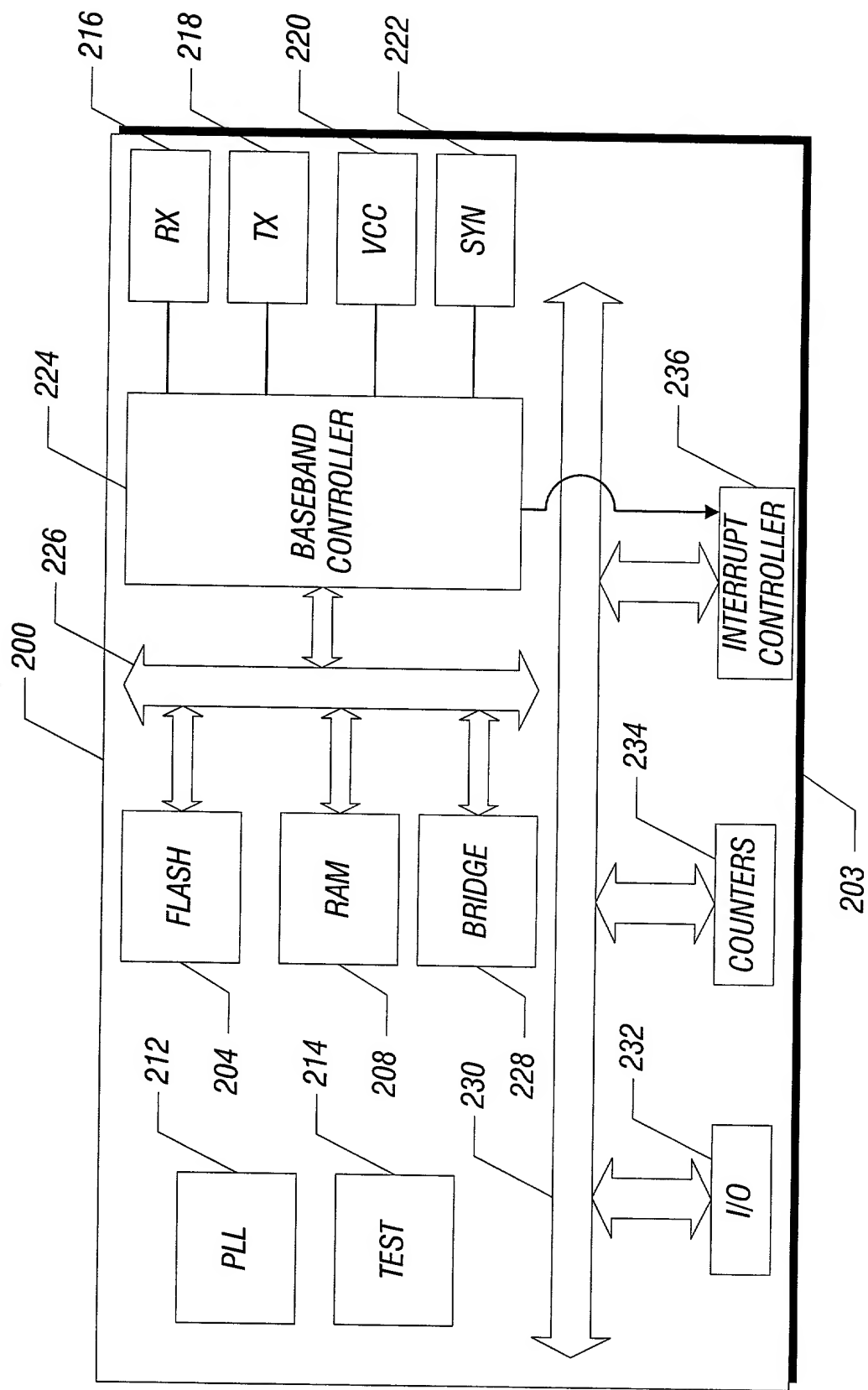


FIG. 21

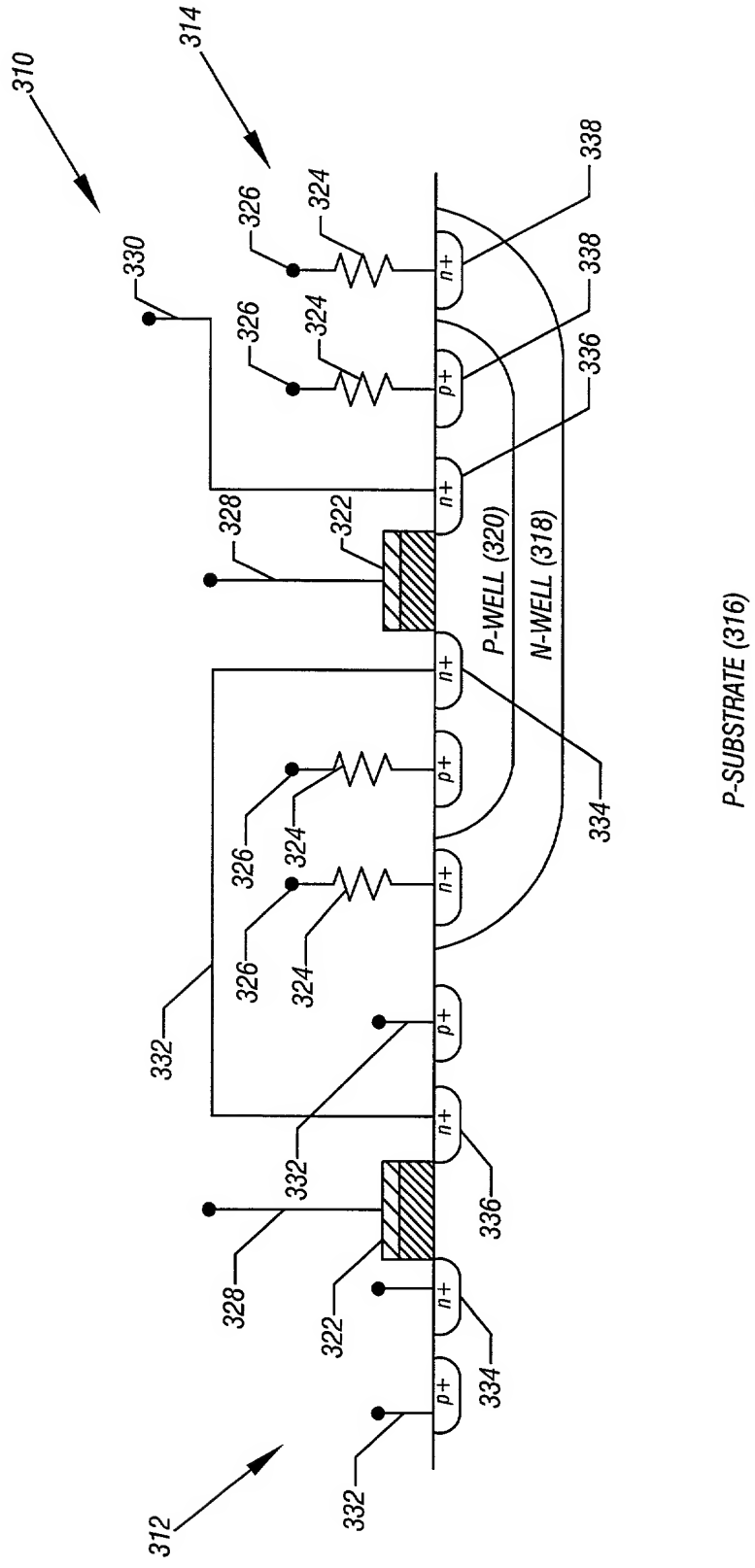
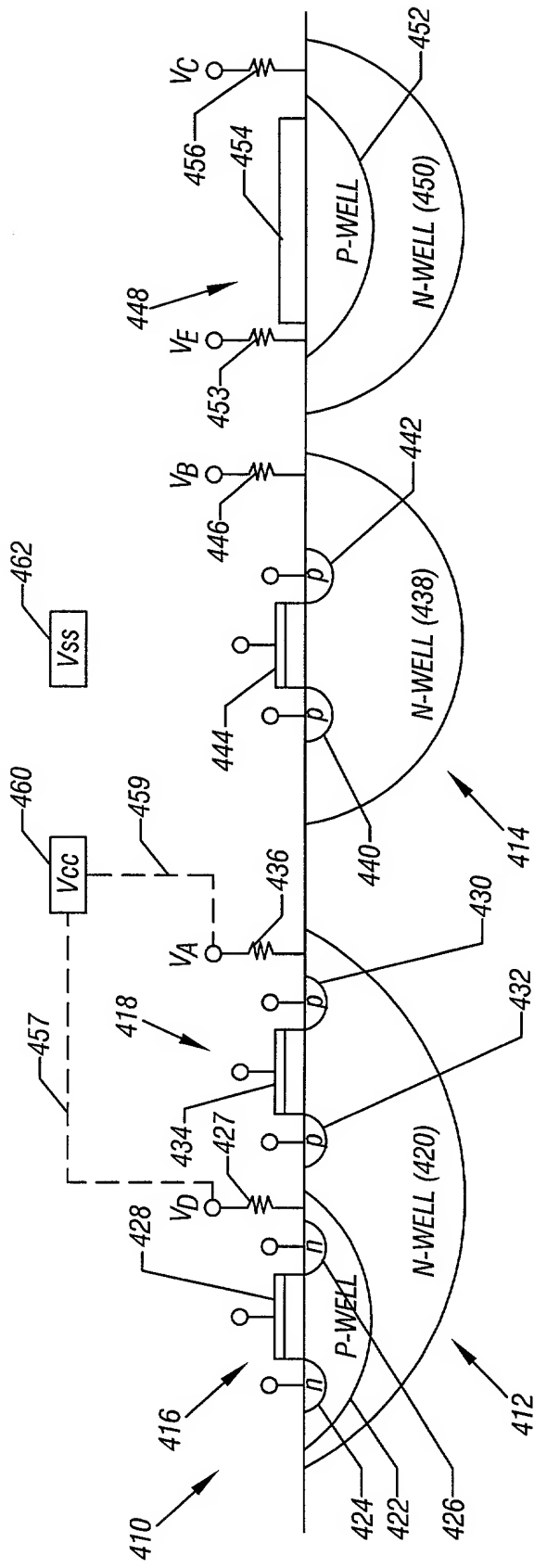


FIG. 22



P-SUBSTATE (448)

**FIG. 23**